| UNIVERSITAT POLITÈCNICA DE CATALUNYA | | | | | | | | | | | | |
|---|---|-----------------------|-----|-------------|----------------------|----------------|--|--|--|--|--|--|
| ESCOLA UNIVERSITÀRIA D'ENGINYERIA TÈCNICA INDUSTRIAL DE BARCELONA | | | | | | | | | | | | |
| | Degree in ENGIN | EERING | i (| All degrees | s) | | | | | | | |
| Escola Univers Tècnica Indust Consorci Escola UNIVERSITAT PO |) | * <u>*</u> Е С т S | | | | | | | | | | |
| Subject: | Programmable | devices | s f | for control | and automation | | | | | | | |
| Acronym: | PDCA | Туре: | | | Optional | | | | | | | |
| Code: | | Semest | er | : | SPRING | | | | | | | |
| Year: | 2011 | Level: | | | | | | | | | | |
| Credits: | Total credits ECTS: | 6 | | Total hours | | 10 2 | | | | | | |
| | In Classroom credits (Theory): | 1,2 | | | oom hours (Theory): | | | | | | | |
| | In classroom credits (Problems): | | | | om hours (Problems): | 1 | | | | | | |
| | Laboratory credits: Guided Activities credits: | 0,6 | | Laboratory | tivities hours: | 1,2 | | | | | | |
| | Out of the classroom credits: | 3,6 | | | classroom hours: | 4 | | | | | | |
| Coordinator: | R. Benítez | -,- | | | | | | | | | | |
| Teaching staff: | R. Benítez, J.M. Guerrero | | | | | | | | | | | |
| | | | | | | | | | | | | |
| Consulting timetable: | | | | | | | | | | | | |
| Prerequisites: | | | | | | | | | | | | |
| Co-requisites: | | | | | | | | | | | | |
| General objectives: | The main aim of the course is to introduce programmable logic devices (PLD's) as a practical tool for implementing digital systems such as digital signal processors and digital controllers. The course will introduce VHDL as the programming language for the design, implementation and test of digital systems. At the end of the course, students are expected to design, implement and test a digital system in areas such as control automation or signal processing. | | | | | | | | | | | |
| Specific objectives by | | | | | | | | | | | | |
| topic: | Unit 1: Describe the main technical features of programmable logic devices. Describe today's most relevant technologies for the implementation of the programmable elements. Select a PLD for a certain practical application based on design, functional and technical considerations. | | | | | | | | | | | |
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| | | | | | | | | | | | | |
| | Unit 2: | | | | | | | | | | | |
| | Design an electronic digital system. Describe the main features of the VHDL language for synthetising digital systems. | | | | | | | | | | | |
| | Implementing digital systems using VHDL. | | | | | | | | | | | |
| | Unit 3: | | | | | | | | | | | |
| | - Describe the main features of DSP's and their architecture | | | | | | | | | | | |
| | - Select a data coding arithmetic system for a certain digital application. Unit 4: | | | | | | | | | | | |
| | Describe the structural and functional components of a digital signal processing ur Describe the structural and functional components of a digital control system. Design and implement a digital signal processing unit. | | | | | | | | | | | |
| | - Design and implement a digital control system. | | | | | | | | | | | |

| Cross competence | s: | | - - - | Pro Lea | arn t | -base o dev | velo | earnir p a p eerin | roje | | | laboi | rative | e fran | newo | rk | | | | | | |
|--|--------|--------|-------------|------------|-------|----------------|------|--------------------------|------|-----|----|--------|--------|--------|--------|----|----|----|----|----|----------|---|
| Topics of the course: | | | | | | | | | | | | | | | | | | | | | | |
| Unit 1: progra | amn | nabl | e lo | gic o | devi | ces (| (PLI | D's). | (7.5 | h) | | | | | | | | | | | | |
| Introduction to PLD's. Classification and types: PLD's, CPLD's and FPGA's. Internal architecture and operation. Technologies of the programmable elements: EPROM, RAM, FLASH. | | | | | | | | | | | | | | on. | | | | | | | | |
| Unit 2: Design and implementation of digital systems. (7.5 h) | | | | | | | | | | | | | | | | | | | | | | |
| Logical Synthesis of automatic machines. Digital systems design with CAD tools. VHDL Programming. Designing and testing applications in programming devices. Designing control process units. | | | | | | | | | | | | | | | | | | | | | | |
| Unit 3: Digital signal processors (DSP's). (7.5 h) | | | | | | | | | | | | | | | | | | | | | | |
| Internal architecture of DSP's. Fixed point arithmetic and floating point. A/D and D/A data conversion. | | | | | | | | | | | | | | | | | | | | | | |
| Unit 4: Implementation of discrete systems in time. (7.5 h) | | | | | | | | | | | | | | | | | | | | | | |
| Introduction to digital signal processing and digital control systems. The z-transform. Digital filters. Implementation of digital PID controllers. | | | | | | | | | | | | | | | | | | | | | | |
| Laboratory: | | | | | | | | | | | | | | | | | | | | | | |
| Designing and implementing applications with FPGA devices. (2h) Designing applications in VHDL: structural architectures. (2h) Designing applications in VHDL: behavioral architectures. (2h) Introduction to digital PID controllers: DSPs, FPGAs. (4h) Design of a hybrid control system based on DSP and FPGA. (4h) | | | | | | | | | | | | | | | | | | | | | | |
| Guided activities: | | | | | | | | | | | | | | | | | | | | | | |
| Design of a digital control system/digital signal processing unit. VHDL implementation and testing using a programmable logic device. Student's Weekly work expressed in hours: | | | | | | | | | | | | | nable | | | | | | | | | |
| Activity /weekly | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | Total | |
| Theory | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | | | | | | 30 | |
| Practice ¹ Problems | 1 | 2 | 1 | 2 | 1 | 2 | 1 | 2 | 1 | 2 | 1 | 2 | 1 | 2 | 1 | | | | | | 14 | |
| Out of the classroom ² | 1 2 | 1 4 | 1 4 | 1 4 | 1 | 1 4 | 1 | 1 4 | 1 | 1 4 | 1 | 1 4 | 4 | 1 4 | 1 4 | | | | | | 15 58 | |
| Practice report delivery ³ | | | | | | | | | | | | | | | | | | | | | | |
| Oral/written tests | | | | | | | | | | | | | | | | | | | | 3 | 3 | 1 |
| | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | | | | | | 30 | |
| TOTAL | 7 | 11 | 9 | 11 | 9 | 11 | 9 | 11 | 9 | 11 | 9 | 11 | 9 | 11 | 9 | 0 | 0 | 0 | 0 | 3 | 150 | 1 |

¹ The laboratory sessions are two hours biweekly, starting the first week. The odd groups attend the 7 sessions on weeks 3, 5, 7, 9, 11 and 13, while

even groups attend to them on weeks 6, 8, 10, 12 and 14. ² This includes the individual out of the classroom activity (learning time) ³ The practice reports entail the work of reduced groups during the whole semester. Each report delivery requires three hours of work (previous preparation of the practice and of the report afterwards).

Teaching/Learning method:

Lectures, practical classes, laboratory sessions.

Project-based learning. Collaborative learning.

Main bibliographic resources:

- 1. A.K. Sharma, "Programmable logic handbook PLDs, CPLDs and FPGAs". Ed. McGraw Hill, 1998).
- 2. Discrete-Time Control Systems, K. Ogata (Prentice Hall, 2nd edition, 1995).
- 3. "Xilinx Synthesis Technology (XST) manual", http://www.xilinx.com/literature.

Complementary bibliographic resources:

- F. Pardo, J.A. Boluda, "VHDL. Lenguaje para síntesis y modelado de circuitos" (Ra-Ma, 1999).
- J.P. Deschamps, J.M. Angulo, "Diseño de sistemas digitales" (Paraninfo, 1992).
- E. Mandado et al. "Dispositivos Lógicos Programables" (Thompson, 2002).
- S. A. Pérez et al. "Diseño de sistemas digitales conVHDL" (Thompson, 2002).

Assessment and qualification:

Follow-up exercises: 25% Final exam: 25% Laboratory: 25% Digital systems project: 25%